R22

Code No: 183AP

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, December - 2024 /January - 2025

DIGITAL ELECTRONICS

(Common to CSE, IT, CSIT, CE(SE), CSE(CS), CSE(DS), CSD)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of **ten questions** (numbered from 2 to 11) **carrying 10 marks each**. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A

(10 Marks)

1.a)	Convert $(235)_{10}$ into hexadecimal numbers.	[1]
b)	Define duality property.	[1]
c)	Simplify A+AB+A'+B.	[1]
d)	What are Universal Gates? Why are they called so?	[1]
e)	Give the difference between encoder and decoder.	[1]
f)	Define de-multiplexer.	[1]
g)	Define clocked sequential circuit.	[1]
h)	Define hold time.	[1]
i)	What is meant by 'static' and 'dynamic' memories?	[1]
j)	What is programmable logic array? How it differs from ROM?	[1]

PART- B

(50 Marks)

2.a)	Verify expression (AB+C+D)(C'+D) (C'+D+E) = ABC'+D.	
b)	Perform (1110111000)-(001100010) by using 1's complement method.	[5+5]

OR

3.a)	Express f(a,b,c) = a+b'c as sum of minterms and canonical form.	
b)	Simplify the Boolean expressions to minimum number of literals i) (A + B)(A + C')(B' + C') ii) AB + (AC) ' + AB'C (AB + C).	[5+5]
4.a)	Using K-map method, Reduce the following Boolean function F=∑m(0,2,3,6,7) + d(8,10,11,15) and obtain minimal SOP.	
b)	Plot the following logical Expression on a 4-variable K –map F=ABCD+AB'C'D'+AB'C+AB and realize the SOP using only NAND gates.	[5+5]

OR

5.a)	Simplify the following Boolean function F, using Quine Mccluskey method F(A,B,C,D)=∑m(1,2,3,7,8,9,10,11,14,15).	
b)	Simplify using K-Map A'B'C'D'+A'CD'+AB'D'+ABCD+A'BD.	[5+5]

6.a) Explain Full binary subtractor in detail.
b) Design a 5 to 32 decoder using one 2 to 4 and four 3 to 8 decoder ICs. [5+5]

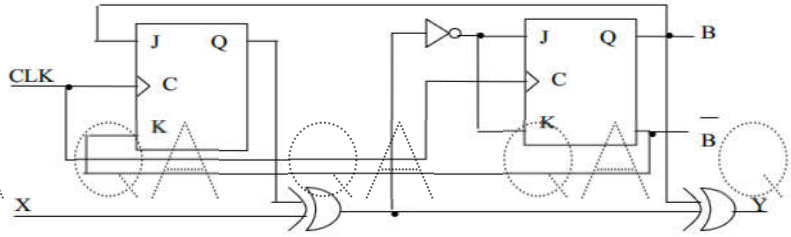
OR

7.a) Describe the operation of 3-bit magnitude comparator.
b) Design a 4:1 multiplexer circuit. [5+5]

8.a) Design a J-K counter for the states 3, 4, 6 , 7 and 3.
b) Design MOD 6 counter using T flipflop. If the clock frequency of the counter is 10MHz, find the output frequencies generated by the flipflops. [5+5]

OR

9.a) Explain the operation of 4 bit universal shift register.
b) A sequential circuit shown below has two JK Flip-Flops, one input X, and one output Y. Derive the state table and state diagram of the circuit. [4+6]



10.a) Design full adder using PAL.
b) A combinational circuit is defined by the functions $F_1 = \Sigma m(3,5,7)$, $F_2 = \Sigma m(5,6,7)$ Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 outputs. [4+6]

OR

11.a) Design and explain a 32×8 ROM.
b) Design a circuit that has no static hazards and implement the Boolean function $F(A,B,C,D) = \Sigma (0,2,6,7,8,10,12)$ using AND-OR logic. [4+6]

---ooOoo---